TITLE: NRAM Neutron Microsensor

PURPOSE

The purpose of this invention is to efficiently sense the presence of thermal neutrons, such as those produced in the vicinity of a nuclear weapon, with a digital electronic neutron counting device capable of counting over long times with little expenditure of power.

BACKGROUND

Owing to their lack of charge and small mass, neutrons cannot be directly measured in any device that is both economical and efficient. Their existence was predicted prior to their discovery by Chadwick, who used a visible scintillator and dark adapted eye for detection. Scintillation remains a major method of detection. Typically the scintillator is coupled to a photomultiplier tube to render an analog electrical signal. Common scintillators are either solid or liquid. The phenomenon of scintillation is the result of electronic transitions which occur in the wake of energetic charged nuclei released by reactions between the incident neutrons and the irradiated atomic nuclei. Other detection schemes involve measuring the charged particles themselves, or the electrons that are liberated in their wake. A surface exposed to neutrons can emit charged particles, including the nuclear reaction products as well as the electrons produced as these nuclei transit the material. These electrons may also be collected within the volume of the irradiated material, whether gaseous or solid. For gaseous detectors, the common method of detection relies on avalanche breakdown of the gas in a high electric field; the signal is collected on one of the electrodes. Semiconductors are favored materials for solid state detectors, as they support an electric field while also allowing charges to migrate to a collection electrode. Semiconductor detectors may operate in an avalanche or non-avalanche mode.

The efficiency of any neutron detector is heavily dependent on the cross section of the material used to convert neutrons to detectable particles. These cross sections depend on the energy of the neutron, and in general are higher for low neutron energies. The inelastic scattering cross sections for neutrons are higher for the light elements. Thus, a neutron beam directed into a thick sample of low atomic number material like polyethylene will undergo considerable scatter from hydrogen atoms, resulting in a thermal neutron gas in which the energy of the individual neutrons is low and their direction is random. The capture cross sections for thermal neutrons are also typically greater for the light elements. The highest capture cross sections for thermal neutrons for (n,alpha) reactions are held by the isotopes Helium 3, Lithium 6, and Boron 10. This accounts for the use of pressurized He-3 gas detectors for thermal neutron detection. It has been recently demonstrated by USNA[1] and verified by NIST that the most accurate quantitation of the measurement of thermal neutron background levels is accomplished with a Helium 3 gas tube, the inner surface of which is coated with a sufficiently thick layer of ^{10}B.

Nuclear weapons give rise to several applications for highly sensitive neutron detectors, such as safeguarding nuclear materials and weapons, treaty verification, anti-proliferation, and the recovery of downed military payloads. Recognition of the need to prevent nuclear smuggling and perform neutron surveillance has gained impetus since the attacks of Sept. 11. Portal monitors, formerly a consideration for regulated facilities, are now an issue for major sporting

events. There is also concern about nuclear security in the various modes of transportation and shipping.

The topic of radiological weapons has also become a concern. Radiological weapons were considered even in World War II, but were not implemented. It is now recognized that there are international terrorists who would consider using radiological weapons. Radiological weapons may not emit neutrons. Thus, a neutron sensor will not detect many types of radiological weapons. Gamma ray sensors have greater capability against radiological threats.

Fundamental, non-negotiable physical properties of the nuclides place limits on the range from which neutron-emitting nuclear materials are detectable. The known decay rates of the relevant isotopes, and the R^2 dependence of signal strength, lead quickly to the conclusion that detection ranges are short, even when using an *ideal* detector of affordable size and integrating over a reasonable length of time. This conclusion becomes even more compelling when the effects of the thermal neutron background is folded in: independent of the detector, emissions from a point source soon fall below the level of the ambient background at a distance R_b, at which point signal recovery becomes more difficult, even for the hypothetical ideal detector. This short detection range becomes a limiting design parameter for any system intended to perform neutron surveillance over any appreciable area, for example a port, a facility, or a transportation hub. The cost per unit area to perform surveillance is dependent on factors such as detector range, detector unit cost, data acquisition cost, reliability, maintenance, manning and operation costs. These factors favor robust, reliable, low cost, networked, unmanned detectors placed within R_b of each other. For example, for a neutron point source of 10^5/sec and an ambient thermal background[1] of 6/(cm^2 hr), R_b is only 22 meters. Clearly, if any appreciable area is to be surveilled for neutrons by deployed sensors, those sensors will need to be closely spaced and inexpensive.

With the advent of solid state electronics, it was realized that a silicon device could be used as a detector for the alpha particle resulting from an (n,alpha) reaction within a converter foil. Initial demonstrations used free standing converter foils placed near a silicon detector such as a PIN diode. More common now are films of converter material placed in contact with or deposited directly upon semiconductor detectors. Even lithium metal has been used for this purpose, although chemical reactivity of the lithium metal leads to a short life for the detector.[2] Greater life has been obtained with compounds of lithium such as LiF, a hard crystalline material. Boron metal has also been applied directly to silicon devices.[3]

Several workers have used neutron converters in conjunction with PIN diodes. In general, the impetus for developing these detectors is for laboratory studies or monitoring power reactors where neutron flux levels are high. The internal noise level of an uncooled diode is appreciable, and consequently they are unable to measure the low background levels of thermal neutrons in the ambient. The typical diode also has a thick semiconductor layer in which charges are collected. Charges liberated by gamma rays are also collected by this layer, and contribute to the non-neutron signal of the device.

There have been research attempts to construct neutron sensing diodes directly from neutron-converting semiconductor compounds. Boron carbides and aluminum dodecaboride have

been investigated, although this work remains experimental.[4]

Boron also finds use in the semiconductor industry as a dopant and in boron containing glass as a passivation layer used to encapsulate the finished chip. It has been demonstrated that the ^{10}B in the dopant or borophophosilicate glass (BPSG) passivation layer is responsible for sensitizing the circuit to neutron irradiation.[5] A favored circuit for testing purposes is the random access memory (RAM) because the effects of irradiation can directly result in bit errors in the stored information. The importance of memory integrity is readily appreciated, particularly in civilian and military computers, avionics and satellite applications in space. A radiation-induced bit error is known as a soft error if the affected memory cell subsequently responds to write commands. In contrast, in a hard error, subsequent attempts to change the state of the cell are ineffective. Both hard and soft errors are known as single event upset (SEU) or single event error (SEE), provided a single incoming particle produces the effect in the cell. Several workers have measured SEU in dynamic RAM (DRAM) circuits. Some workers have attempted to coat commercial DRAM circuits with a converter, in order to use SEU as a neutron detector. In some cases, the top of the package of the DRAM has been removed and the boron coated on the passivated chip. Some workers have proposed further milling to remove the passivation layer from the top of the chip before adding the converter film. These efforts to date have resulted only in insensitive detectors. DRAM circuits require frequent powered refreshing of the stored information.

SEU can be caused by various types of incoming particles. Much of the work on the hardening of microcircuitry for space applications has centered on ion bombardment, because energetic ions are plentiful in space, can be penetrating, and need no converter to induce an effect. Proton bombardment has also been investigated; protons can undergo nuclear reactions in the irradiated material, liberating ions that can cause upsets. Alpha particle and neutron irradiation of microcircuits have also been studied. The design of memory circuits, and the process technologies used to make them, have evolved to enhance the radiation hardness of memory cells.

Investigation of susceptibility to SEU has revealed an important quantity called the critical charge Qcrit, which is the amount of charge the memory cell must accumulate in order to produce a bit error. It has long been known that finer lithographic linewidths lead to smaller cells, to smaller cell capacity to hold charge, and thus to smaller Qcrit.[6] This is depicted for unhardened memory chips in Figure 1.

DESCRIPTION AND OPERATION

We desire a detector that does not require gas fill or high voltage, is insensitive to thermal noise in silicon or other leakage currents, is insensitive to gamma rays, and is sensitive to single neutron events. This permits the counting of individual neutron events, rather than the accumulation of aggregate charge (including thermal noise) from multiple neutron events as is done with diodes. These goals are accomplished with a RAM detector with a Qcrit small enough for single neutrons to use a converter to induce single event upsets (SEU). From Figure 1, we can determine the linewidth required to achieve this goal by direct deposition of charge in a RAM cell of known dimension. Whereas DRAMs require refreshing due to accumulation of leakage

current and CCDs require periodic cycling to flush out accumulated dark current, this issue has been solved for Static RAM (SRAM) circuits, which hold their memory state indefinitely with very little investment of power (of order one microamp). We achieve our goals with a Neutron-sensitive SRAM (NRAM), described below.

Figure 2 shows the cross section of a Honeywell silicon-on-insulator (SOI) 4MB SRAM. The device was sectioned prior to application of the passivation layer, which would be applied on top (see figure). The active silicon layer is only approximately 200 nm thick, and is located near the bottom of the figure (see markers on figure). It is this layer which the neutron-generated alpha particle must transit in order to deposit charges in that layer and produce an upset. The structures above the active silicon layer are the circuit levels required to achieve the RAM functionality. The figure further indicates the range of an alpha particle resulting from a neutron reaction with a ^{10}B atom. Clearly the thickness of the circuitry is greater than the alpha range in silicon. There would be a large range discrepancy encountered by alphas emitted by a boron converter placed on top of the circuitry layers. The discrepancy is even larger than depicted, particularly if the converter were to be placed atop the passivation layer. This illustrated device design is actually relatively simple; other RAM designs may have two to three times as much material in the circuitry structure, with even greater thickness through which an alpha must pass to reach the active silicon. Clearly the converter should not be placed so far away from the active silicon, as the alpha energy will be dissipated before it reaches the active silicon. This explains the low sensitivity achieved in previous work with DRAMS: converter layers were on top, too far away.

nuclear force size - cross section

A key feature of the present device is that the converter layer will be placed close to the active silicon layer, forming a Neutron-sensitive RAM (NRAM) sensor. By close we mean that the converter may be in contact with the active silicon, or separated from it by an insulating layer and/or a diffusion barrier layer. Typical dimensions for these layers are in the hundreds of nanometers.

The 200 nm thickness of active silicon in an SOI device is much less than the range of the alpha particle. Thus, only a fraction of the alpha energy will be deposited in the active layer. The relevant quantity then becomes the amount of energy deposited along the track of the alpha, i.e., the Linear Energy Transfer (LET). The LET of an alpha from ^{10}B traversing silicon is plotted[7] in Figure 3. It is seen that the LET varies from about 1 to 1.5 Mev/(mg cm^2) over essentially the entire useful energy range of the alpha. Applying these limiting values to a 200 nm thickness gives the range of energy deposited in the active silicon for normal incidence (the charge will increase for non-normal incidence with greater path lengths through the active silicon). From Peterson,[6] the energy (in MeV) required per liberated charge (in pC) is 22.5, giving a value of about 2 to 3 femtocoulombs deposited in the active layer at normal incidence. Figure 1 is replotted as Figure 4, now including these limiting values for liberated charge in the active layer.

It is seen from Figure 4 that a ^{10}B alpha, at almost ~~any point in its trajectory in silicon~~, will supply an amount of charge comparable to Qcrit for a 0.35 micron linewidth SOI RAM cell. The linewidth of the SOI RAM circuit depicted in Figure 2 is, in fact, 0.35 microns. Finer linewidths down to 0.13 micron are being fabricated by other semiconductor foundries, notably IBM, for which linewidths the alpha would deposit an amount of charge in excess of Qcrit. In other words, a proximally placed ^{10}B converter will produce alphas capable of causing SEU in

the SOI SRAM.

The optimal thickness of the converter can be calculated.[7] The benchmark converter thickness is that thickness for which the product of neutron absorption within the converter and alpha emission from the converter is a maximum. For a ^{10}B converter, this thickness is 1.8 microns. For converters of other composition, the same type of calculation may be performed but the optimal thickness will generally differ for each converter composition.

The composition of the converter may be boron metal enriched in the isotope ^{10}B, although the metal must be separated from the silicon by an insulating layer. A 200 nm layer of silicon oxide will suffice to provide the required insulation between the boron and the silicon, see Figure 5. Boron layers have been placed directly on silicon diodes by McGregor,[2] who has shown that mechanically stable films of the required thickness can be achieved provided that provision is made for stress relief. It is well known that borosilicate phosphate glass (BSPG) is compatible with application on silicon devices, and is commonly used for passivation layers. A BSPG glass with 5% boron may be applied directly to the chip. The composition of such glass is widely variable in terms of its boron content. Boron compounds and compositions may also be used. Converters may also incorporate the lithium ion, such as a layer of LiF which is a stable material. Lithium metal is highly reactive and has been used by others to sensitize diodes, but with short sensor life.

For the converter to be in proximity to the active silicon of an SOI SRAM, fabrication of the converter layer may be done prior to or after circuit manufacture.

The converter material may be added to the SOI *substrate* prior to fabricating the circuit, in a manner that insures that the converter will be near the active silicon and the thin buried oxide (BOX) region of the completed device. A modified bonded silicon technique is used, in which an oxided first silicon wafer is bonded to a second silicon wafer called the handle wafer. After a thinning process carried out on the first wafer, the active silicon becomes accessible. At this point, the bonded assembly has become an SOI substrate, and the circuit is fabricated upon its silicon layer. The handle wafer merely provides mechanical stability for the completed circuit, thus the name. The modification we make to the normal bonded-silicon process is this: a ^{10}B enriched film is deposited over the handle wafer before bonding. Bonding takes place between the oxided first wafer and the converter layer on the handle wafer. After thinning the first wafer, the result is an SOI wafer with converter layer beneath the oxide layer. Containment of the boron within the BOX region during processing of the wafer is necessary to prevent unwanted doping of the top active silicon film. Also, out-diffusion of the converter material into the fabrication tools needs to be prevented; the use of nitride diffusion barriers suffice. This converter-sensitized SOI substrate wafer is then put through standard CMOS fabrication processes to build large quantities of SRAM circuits that will serve as neutron detectors.

A second method for placing the converter layer in proximity to the active silicon is carried out on the chip or wafer after the circuit has been fabricated in the usual fashion (i.e., not using the pre-loaded SOI substrate just described). The chip or wafer is first bonded on the top side (the side holding the circuitry) with a thick material such as epoxy to provide mechanical stability to the circuit during subsequent handling and processing. The back of the wafer is then

processed to remove the wafer up to the BOX layer. Lapping or similar processes are suitable for removing of an initial thickness of wafer, leaving sufficient thickness to avoid removing the BOX layer itself. The remaining thickness can be etched with etchants that stop at the BOX, such as hydrazine. With the wafer now removed, a layer may be applied to the BOX to prevent converter diffusion (may not be required if the chip experiences no elevated temperatures hereafter), and the converter layer may then be applied. Sputter coating will produce lower thermal stresses in the circuit during the deposition process, and is to be preferred for fragile circuits. The converter having been applied, the circuit will now perform as a thermal neutron sensor. Additional stable material such as epoxy may be applied if needed for mechanical stability.

One notable application for the NRAM is the monitoring of transportation cargo. We calculate that NRAM chips with a total sensitive area of 4 cm^2 may be mounted on one end of a 20 foot shipping container and detect (5 sigma) a 10^5 neutron source at the far end in just over 2 hours. Increases in ambient background of 4x have only a minor effect on counting times at this distance. The low standby current draw (microamp) of the NRAM allows integrations of any desired duration to be performed without difficulty. Battery life can be many years. The NRAM is compatible with digital circuitry, such as that used by satellite tags being employed by commercial shippers for logistic tracking. Some of these tags have an unattended battery life of years with reports every 4 hours, include receivers to prompt reporting or other actions, contain programmable digital signal processors capable of reading the NRAM, report geo-location and provide global data transfer. The NRAM has obvious application to global nuclear security in the transportation industry, whether on shipping containers, trucks, ports, terminals, or hubs.

The NRAM can similarly be used for mobile or relocatable tags for nuclear security concerns other than transportation. For example, a building, facility, or wide area can be instrumented with NRAM sensors. Data acquisition can proceed through satcomm, as above, or though a wireless network such as a Bluetooth net, or through a wired system. For military special operations, the NRAM can be clandestinely deployed and remain on station for years, giving reports daily, upon request, or upon event.

RAM circuits are semiconductor devices whose circuit design and foundry fabrication follow the mass produced consumer electronics marketplace. The NRAM achieves all these attributes. The NRAM is commercially manufacturable and benefits from the economies of scale in the semiconductor memory market.

Multiple NRAM chips may be combined to increase the speed of data acquisition. Sensors composed of multiple NRAM chips may also be useful as portal detectors. Such multi-NRAM sensors may also serve with active detection systems which stimulate neutron emission, such as are currently under investigation for cargo inspection, provided a neutron moderator (such as polyethylene) is placed nearby to thermalize fast neutrons which may be produced.

It is well known that ambient neutron backgrounds vary diurnally (a few to several percent) and with lattitude and altitude. There are variations due to solar events. These global quantities are monitored continuously and are published, for example by NOAA. In certain instances, these variations may be taken into account to insure proper data interpretation. The

continued ability of the NRAM to detect ambient background levels is a positive indication that the device is functioning. The level of measured background may in some instances be suitable for operational calibration of the device in situ.

ADVANTAGES AND NEW FEATURES

Silicon microcircuits are known to be durable to the extent that they can be packaged into artillery shells and function during a 50,000 g launch, during trajectory, and after recovery. The NRAM is robust and durable.

The holding current of SOI SRAMs (1 microamp or less) is compatible with years of battery life.

The NRAM is a solid state device and is capable of unattended remote operation, requiring no operator.

The NRAM is a digital circuit, directly compatible with communication and computer technologies.

The NRAM is a threshold event detector in which individual neutrons cause a local threshold crossing in a memory cell. Thermal noise in the detector is below threshold for normal operating temperatures. (Temperature excursions affecting the NRAM will also affect the circuits required for readout and reporting; the NRAM introduces no new environmental limitations.)

The NRAM is not sensitive to ambient pressure.

The NRAM can integrate for short or long times. Integration time is not limited by accumulation of dark current or leakage current.

The NRAM is a sensitive neutron detector, capable of measuring ambient background.

The NRAM contains no liquids or gases, and needs no replenishment other than very infrequent battery replacement (years).

The NRAM is manufacturable with the mass production processes of the silicon foundry, and benefits from the economies of scale of the computer memory market.

The initial design of the NRAM circuit is a modification of commercial mask sets, which is considerably less expensive than a complete redesign of all masks.

ALTERNATIVES

Converters may be of various compositions, including ^{10}B, BPSG of a range of boron compositions, other boron compounds and compositions, and lithium-6 compounds or compositions.

An additional SRAM circuit can be applied to the single-sided NRAM to produce a sandwich sensor, the center layer of which is the converter, on either side of which are SRAM cicruits. The technology has already been demonstrated for multiple stacked layers of silicon microcircuits, and this technology can be advantageously applied to stacked NRAMs. However, with each additional converter layer, there is a diminution of added sensitivity owing to the absorption of neutrons per converter layer.

Multiple converter layers can increase sensitivity. With a back-thinned NRAM in which the converter forms an outer surface (see Figure 6), an additional ^{6}LiF converter can be added to increase sensitivity above that achieved with boron alone.

The NRAM has been described with reference to silicon memory SOI circuits, however other semiconductors may be used to fabricate semiconductor-on-insulator RAM circuits and these can also be neutron-sensitized with one or more proximal converter materials to make NRAM sensors.

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Figures.

Figure 1. Qcrit for unhardened RAM chips, from Petersen.[3] (no boron information)

Figure 2. Cross section of a Honeywell silicon-on-insulator (SOI) SRAM, made with 0.35 micron linewidth lithography. (Courtesy of Honeywell. Honeywell PROPRIETARY.)

Figure 3. LET of an alpha from ^{10}B traversing silicon.

Figure 4. Qcrit plot, now including charge generated in 200 nm thick active silicon layer by passage of an alpha particle from ^{10}B, based on the LET extreme shown in Figure 3.

Figure 5. Diagram of NRAM with boron converter separated from the active silicon by 200 nm of oxide, on the side of the active silicon away from the circuit elements.

Figure 6. Diagram of NRAM with multi-element converter of boron and LiF, each enriched in its respective neutron sensitive isotopes.